WHAT IS CLAIMED IS:

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1		Λ	driver	CITCHIT	comprising:
	1.	$\boldsymbol{\Gamma}$	uiivci	CIICUIL	COMBINISHIE.

- an output transistor connected between a voltage terminal and an
- output node to produce an output signal on said output node, said output transistor
- 4 including a control terminal;
- a current source connected to said control terminal of said output
- 6 transistor to provide a reference current;
- a feedback capacitor connected from said output node to said
- 8 control terminal of said output transistor to control said output transistor as a
- 9 function of a difference between current through said capacitor and said reference
- 10 current.
- 1 2. The driver circuit of claim 1 further comprising a memory operatively
- 2 connected to said control terminal of said output transistor, said memory being
- 3 configured to store a signal on said control terminal of said output transistor from
- a previous operating cycle in which said output transistor was activated.
- 1 3. The driver circuit of claim 2 wherein said memory includes a memory
- 2 capacitor and an amplifier, said amplifier being connected to said memory
- 3 capacitor and said output transistor such that said amplifier is selectively
- 4 configured in a voltage follower configuration to store said signal on said control
- 5 terminal of said output transistor in said memory capacitor.
- 1 4. The driver circuit of claim 3 further comprising a controlled switch located
- between said memory capacitor of said memory and said control terminal of said
- 3 output transistor, said switch comprising a control input connected to said output
- 4 node.
- 1 5. The driver circuit of claim 1 wherein said current source is configured to
- 2 generate said reference current proportional to a reference voltage and a reference
- 3 frequency.

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output node.

1	6. The driver circuit of claim 5 wherein said current source includes a				
2	frequency-to-current converter.				
1	7. The driver circuit of claim 1 further comprising a first switch located				
2	between said voltage terminal and said output transistor and a second switch				
3	located between said current source and said control terminal of said output				
4	transistor, said first and second switches being controlled by an input signal.				
1	8. The driver circuit of claim 1 further comprising:				
2	a second output transistor connected between said output node and				
3	a second voltage terminal, said second output transistor including a control				
4	terminal;				
5	a second current source connected to said control terminal of said				
6	second output transistor; and				
7	a second feedback capacitor connected from said output node to				
8	said control terminal of said second output transistor.				
1	9. A driver circuit comprising:				
2	an output transistor connected between a voltage terminal and an				
3	output node to produce an output signal on the output node, said output transistor				
4	including a control terminal;				
5	a memory connected to said control terminal of said output				
6	transistor, said memory being configured to store a signal on said control terminal				
7	from a previous operating cycle in which said output transistor was activated;				
8	a current source connected to said control terminal of said output				
9	transistor to provide a reference current; and				

control terminal of said output transistor to control a rate of signal change on said

a feedback capacitor connected from said output node to said

- 1 10. The driver circuit of claim 9 wherein said memory includes a memory
- 2 capacitor and an amplifier, said amplifier being connected to said memory
- 3 capacitor and said output transistor such that said amplifier is selectively
- 4 configured in a voltage follower configuration to store said signal on said control
- 5 terminal of said output transistor in said memory capacitor.
- 1 11. The driver circuit of claim 10 further comprising a controlled switch
- 2 located between said memory capacitor of said memory and said control terminal
- 3 of said output transistor, said switch comprising a control input connected to said
- 4 output node.
- 1 12. The driver circuit of claim 9 wherein said current source is configured to
- 2 generate said reference current proportional to a reference voltage and a reference
- 3 frequency.
- 1 13. The driver circuit of claim 12 wherein said current source includes a
- 2 frequency-to-current converter.
- 1 14. The driver circuit of claim 12 further comprising a first switch located
- between said voltage terminal and said output transistor and a second switch
- 3 located between said current source and said control terminal of said output
- 4 transistor, said first and second switches being controlled by an input signal.

1	15. The driver circuit of claim 9 further comprising:				
2	a second output transistor connected between said output node and				
3	a second voltage terminal, said second output transistor including a control				
4	terminal;				
5	a second memory connected to said control terminal of said second				
6	output transistor, said second memory being configured to store a signal on said				
7	control terminal of said second output transistor from a previous operating cycle				
8	when said second output transistor was activated;				
9	a second current source connected to said control terminal of said				
10	second output transistor to provide a second reference current; and				
11	a second feedback capacitor connected from said output node to				
12	said control terminal of said second output to control a second rate of signal				
13	change on said output node.				
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1	16. A method for driving an electrical device, said method comprising:				
2	receiving an input signal;				
3	applying a stored signal to an output transistor in response to said				
4	input signal to produce an output signal on an output node; and				
5	controlling said output signal on said output node using a				
6	difference between a reference current and current capacitively fed back from said				
7	output node.				
1	17. The method of claim 16 further comprising storing a control signal on said				
2	output transistor as said stored signal.				
1	18. The method of claim 16 wherein said controlling includes generating said				
2	reference current using a reference frequency and a reference voltage, and				
3	applying said reference current to a control terminal of said output transistor.				

- 1 19. The method of claim 16 further comprising:
- applying a second stored signal to a second output transistor in
- 3 response to said input signal to change said output signal on said output node; and
- 4 controlling said output signal on said output node using a
- 5 difference between a second reference current and current through a second
- 6 capacitive feedback from said output node to said second output transistor.
- 1 20. The method of claim 19 further comprising alternately activating said
- 2 output transistor and said second output transistor.